

Quantifying the Impact of Current-Sensing on Interconnect Delay Trends

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Abstract— This work tries to compare the performance of traditionally used repeaters with a recently proposed differential current-sensing signaling technique for present and future technologies. Several technology scaling models have been proposed for device and interconnect scaling. For this study Berkeley Predictive Technology Model, Semiconductor Industry Association model and Sylvester-Keutzer model are used. Percentage chip reached in a clock cycle is used as a metric. This allows a better understanding of the impact of these circuit techniques on architecture and floorplaning issues. Results show that differential current-sensing signaling is significantly faster than repeaters for most of the scaling theories and hence allows for a larger coverage of chip in a clock cycle. If clock rates are scaled more aggressively (as they have been in past), the gains for current-sensing can be even more significant. Any new circuit style presents design challenges and potential power and area tradeoffs. Despite these challenges and as a motivation to overcome them, this paper shows a methodology and preliminary results that indicate opportunities for novel interconnect circuits.

Keywords— Current-sensing, Repeaters, Chip coverage, Technology scaling.

I. INTRODUCTION

Even though integrated circuit performance has improved with successive technology generations (higher levels of integration at greater clock frequencies), the full exploitation of the shrinking feature sizes has not been possible primarily due to certain physical constraints. There exist major technical challenges in dealing with device and interconnect scaling. Extensive studies have been carried out to identify and address the DSM device issues like threshold voltage roll-off, Drain Induced Barrier Lowering (DIBL), increased sub-threshold leakage current etc [1], [2]. It is now a well known fact that as VLSI design advances to DSM technologies, interconnects are going to be a barrier to continued performance gains.

Various approaches have been adopted to counter the interconnect delay problem ranging from suitable choice of materials to alternate circuit techniques (repeater insertion [3], current-sensing [4], [5], boosters [6]) to architectural modifications [7]. Several interconnect scaling, delay and power models have been proposed and various optimizations have been performed to study interconnect delays and minimize their detrimental effect on overall circuit performance [7].

In this paper we study the impact of scaling on in-

terconnect delays for two circuit styles (repeaters, current-sensing). More specifically we aim at projecting the performance benefits of the alternate circuit style over the conventional repeater insertion technique. Studies on interconnect issues have been done earlier in [3], [7], [8], [9], [10], [11] but they have not explored the usage of alternate circuit styles to improve interconnect performance. The metric used to characterize the interconnect delay in this paper is the percent die area covered in one clock cycle [8]. This gives us an estimate of wire delays and the architectural level impacts for future DSM technologies. The National Technology Roadmap for Semiconductors (NTRS) [12] provides a guideline towards predicting the interconnect parameters for future technology generations. Building on the roadmap, there are other scaling theories that have been proposed - some present a pessimistic prediction and the others give a more optimistic overview. A review of some of these predictive models and their relevance to our analysis is presented in Section 2. In section 3 the circuits under test are introduced with an insight into the analysis methodology. The results for the experiments carried out are presented in section 4. Section 5 provides some recommendations based on the observations and certain guidelines for future work on this topic.

II. ROADMAP & SCALING MODELS

The NTRS roadmap [12] is typically regarded as the standard reference for assessing and understanding the requirements of semiconductor technology advancement. It provides a consolidated summary of the key technology metrics and an overview of the future of semiconductor circuit technologies. Most of the scaling models proposed (including those considered in this paper) use this as the basis for developing their predictive methodologies for the parameters that are not explicitly mentioned in the roadmap. The scaling theories differ in the parameters taken into consideration to develop the model. Here we look at three different scaling models and examine the interconnect trends exhibited by each of them.

One of the models, the Semiconductor Industry Association model (SIA model) is adapted directly from the roadmap i.e predictions are a direct fall-out of the proposed fundamental parameters in the NTRS roadmap. A more conservative model has its projections made under assumptions like the dielectric constant not dropping below 2.3, not using materials other than Cu etc [10]. The third scaling model under consideration in the Berkeley Predictive

Technology Model (BPTM) which is a SPICE based tool that determines interconnect parameters using the analytical expressions of interconnect resistance and capacitance [13]. The global interconnect parameter projections are obtained from [10] and [13] for the above mentioned scaling models.

The variation of the interconnect resistance and capacitance per unit length for the above mentioned scaling models are shown Figure 1. Another model that differs significantly from these is the Sylvester-Keutzer model (S-K model) which assumes that global wires are fat and remain unscaled across technology generations [9]. Hence the resistance and capacitance per unit length of the wires remains the same for all technologies.

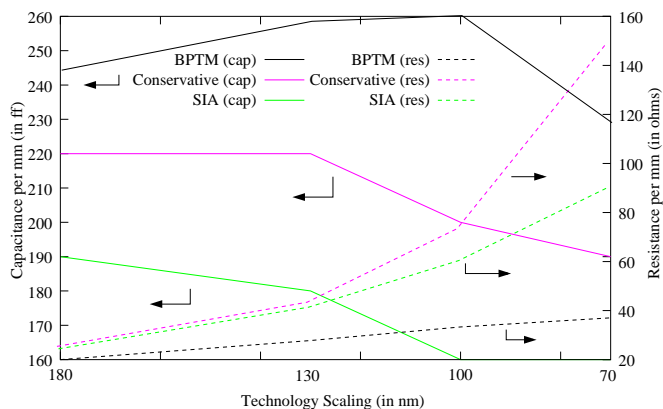


Fig. 1. Resistance and Capacitance per mm for various scaling models

For the exhaustive study on the scaling trends of the interconnects, we use the BPTM projections as they provide the most complete picture of the interconnect behavior including consideration of coupling capacitances with the neighboring lines. The interconnect scaling behavior according to the S-K model is also analyzed. Since the resistance and capacitance per unit length is assumed to be the same for all technologies in the S-K model, the industry interconnect data currently available for the 0.18μ technology (Res. per mm - 60Ω , Cap. per mm - 423fF) is used for the global wires in all technology generations. In order to characterize the interconnect delay in terms of % of chip area covered in a clock cycle, the fact that both the clock frequencies and the die sizes vary with technology has to be considered. The data for these parameters can be directly incorporated from the roadmap. The device scaling has been carried based on the BSIM specifications [14]. A consolidated summary of the parameters of interest is shown in the table below.

III. CIRCUITS UNDER CONSIDERATION

A. Repeaters

Repeater insertion is a classical solution which changes the delay dependence on the wire length from quadratic to linear. Bakoglu in [3] summarizes that the delay of the repeater should be equal to the delay of the interconnect

Technology (nm)	180	130	100	70
Clock (GHz)	1.2	1.6	2.0	2.5
Vdd (V)	1.8	1.5	1.1	0.9
Chip area (mm^2)	340	372	408	468
Res. of min. size inv. ($\text{K}\Omega$)	9.02	10.56	11.37	13.71
Cap. of min. size inv. (fF)	1.795	1.267	0.996	0.709

TABLE I

TECHNOLOGY PARAMETERS - FOR ALL SCALING MODELS

in order to optimally drive the interconnect. This principle is used to find the number of repeater stages and repeater size. A significant amount of work has been done in determining the optimal placement and size of the repeaters [3], [15], [16], [17], [18], [19].

For the purpose of this study Bakoglu relations [3] (Equation 1) are used to determine the number and size of delay-optimal repeaters required to drive a line of given length.

$$k = \sqrt{\frac{0.4R_T C_T}{0.7R_o C_o}}$$

$$h = \sqrt{\frac{R_o C_T}{R_T C_o}} \quad (1)$$

where,

k is the number of repeaters in the repeater chain,

h is the size of each repeater (width of n-device),

R_T is the total resistance of the interconnect,

C_T is the total capacitance of the interconnect,

R_o is the output resistance of a minimum size inverter,

C_o is the input capacitance of a minimum size inverter.

B. Current-sensing

Current-sensing or current-mode determines the logic value transmitted on a wire based on the current through the wire. In current-sensing, the line is terminated by a short, shunting the wire capacitance. By avoiding the charging of the wire capacitance, current-mode systems save dynamic power and time. [4] compares the current-sensing technique with optimal repeater insertion and discusses the advantages and disadvantages of current-sensing.

Both differential [4] and single-ended [5] current-sensing perform better than optimal repeater insertion in terms of delay and power. Since no partitioning was used in the current-sensing method, the delay increased quadratically with respect to wirelength and for very long wire lengths, current-sensing delay was greater than the optimal repeater delay (Figure 2). Current-sensing delay is also very sensitive to the driver size and the delay saturates as the driver size is increased. Static power is significant portion of the total power dissipated and some circuit modifications are required to make it more power efficient. Figure 2 using

0.18 μ shows some achievable results for current-sensing repeaters. For the purpose of this study only unrepeated current-sensing is considered. The usage of current-sensing repeaters is expected to improve the gains further.

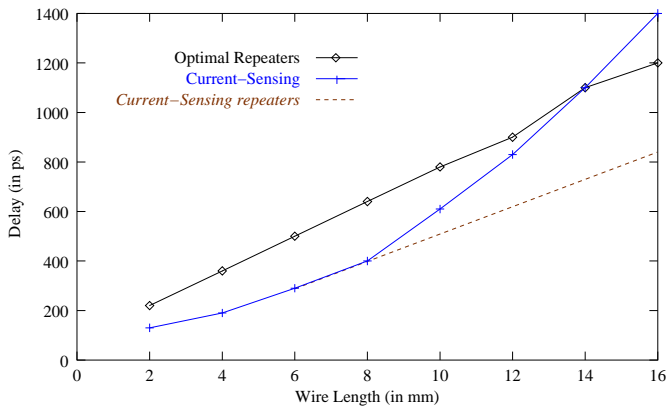


Fig. 2. Comparison of current-sensing with repeaters and a possible result for current-sensing repeaters

C. Circuit model used for simulations

A circuit model of the above mentioned techniques was used to perform simulations. The assumptions used to come up with this circuit model are based on extensive discussions with high performance microprocessor circuit designers at Compaq, Intel and Motorola. For current-sensing a sensing circuit previously proposed (Figure 3 [4]) was used. The setup for the simulation is shown in Figure 4. The wire was modeled as a 5- π distributed RC line.

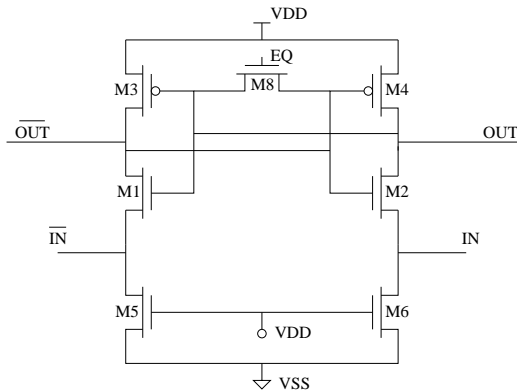


Fig. 3. Modified Clamped Bit-Line Sense Amplifier (MCBLSA)

IV. RESULTS

The key metric used in this study for comparing the delay of various circuit techniques is the percentage of die reached in one clock cycle. The results were generated using automated HSPICE simulations based on the circuits of section 3 and models of section 2. Figure 5 and Figure 6 are the plots of percent chip area covered by the various circuit techniques using BPTM and the S-K models.

Current-sensing and repeaters perform equally well for BPTM, while for the S-K model current-sensing provides

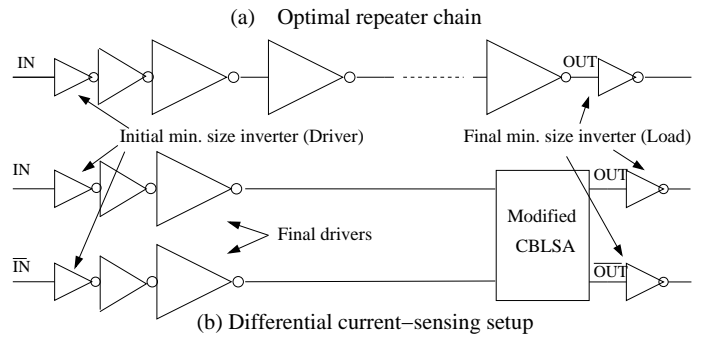


Fig. 4. Setup for the simulation

significant speedup and hence coverage over repeaters.

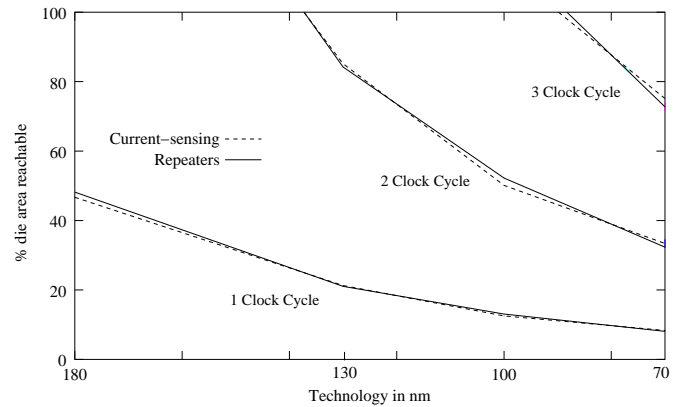


Fig. 5. Percentage of chip reachable using BPTM model

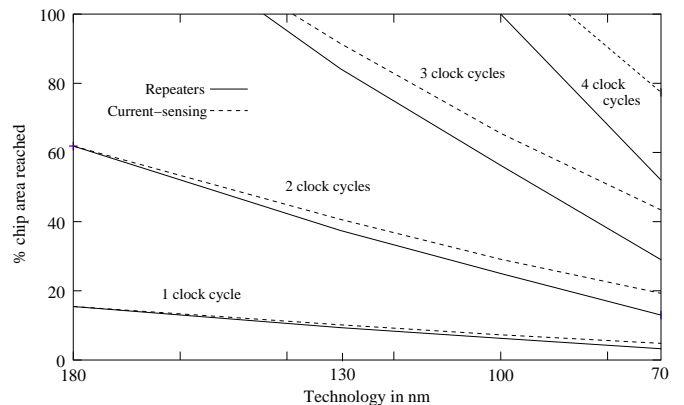


Fig. 6. Percentage of chip reachable using S-K model

A. Results for repeaters

An interesting result of the study was the number of repeaters required for the wires across technology. Figure 7 shows the number of repeaters required per mm of wire length. The number of repeaters required per mm increases as technology scales. However Figure 7 also shows that the number of repeaters in a clock cycle are reducing. This plot is for very conservative estimates of clock frequency,

for ideal process and delay-optimal insertion. If aggressive estimates of clock frequency and process variations are taken into account the number of repeaters per clock cycle is going to reduce significantly. This shows a trend away from very long single-cycle lines in future technologies and these long wires will need to be pipelined to achieve the clock frequency at the cost of higher latency. This also makes a strong case for wave pipelining, multicycle wires and other unconventional timing and signaling techniques. The size of repeaters as the technology scales also increases from 246(x min. size inv.) for 180nm to 345(x min. size inv.) for 70nm, thus encouraging the use of other circuit techniques.

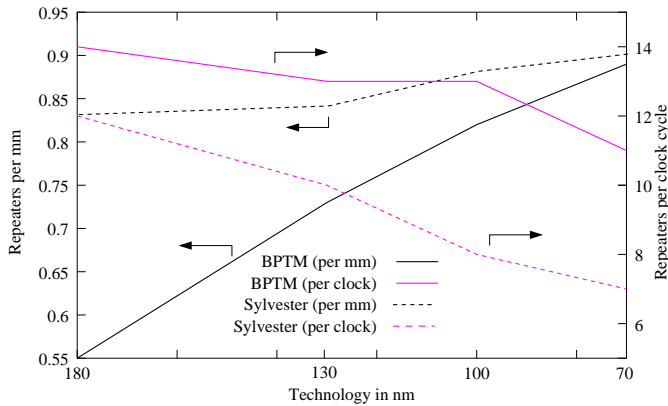


Fig. 7. Number of repeaters required per unit length and per clock cycle

B. Results for current-sensing

As seen from Figure 5 current-sensing shows nearly no gain in the % of chip reached. This is due the fact that the wires for which the delay is approximately one clock cycle are very long. As shown in Figure 2, the delay for unrepeated current-sensing is quadratic with respect to wire-length, so for long lines current-sensing is not very attractive. However if the estimates of clock frequency are aggressive, which will translate into smaller line lengths for one clock cycle, current-sensing method will provide significant performance benefit. Figure 8 compares line lengths driven by repeaters and current-sensing, assuming that half of the clock cycle is taken by the logic.

C. Effect of inductance on chip coverage

The simulation results for the % of chip reached discussed in the previous subsections are based on RC wire models. It has been shown that while modeling global interconnects, inductance cannot be ignored[20], [21], [22]. It is predicted that in future technologies the effects of self and mutual inductance will be more prominent. To study the effect of inductance on chip coverage, simulations for BPTM technology models were performed with the self and mutual coupling of the interconnect included. As shown in Figure 9 differential current-sensing outperforms repeaters significantly.

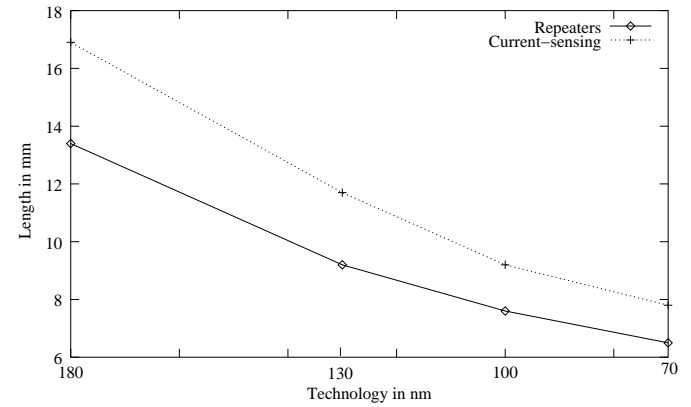


Fig. 8. Line lengths driven by current-sensing and repeaters assuming that half of delay is taken by the logic

Since differential signaling is used for current-sensing, neighboring wires always have opposite AC currents. This limits the magnetic fields between the neighbors and hence results in less effective inductance. Differential voltage-sensing would also benefit from this fact and the wire will have very little effective inductance[22]. However, differential voltage sensing is slowed down significantly due to the coupling. Since current-sensing does not allow the wire capacitance to get charged, coupling capacitance has little impact on current-sensing. Thus differential current-sensing provides a solution which is insensitive to capacitive and inductive coupling.

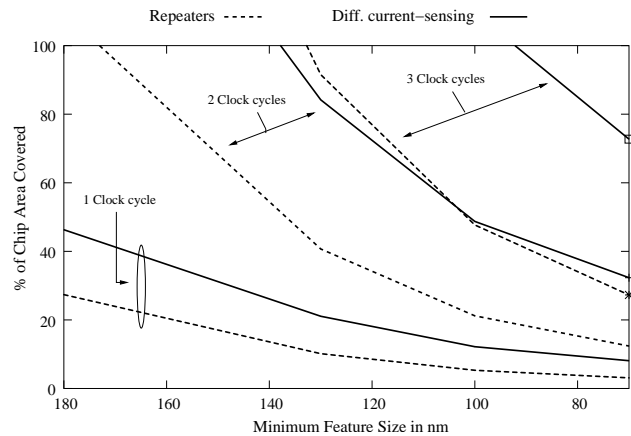


Fig. 9. Percentage of chip reachable using BPTM model with inductance

D. Discussion of power and secondary issues

A significant amount of power in current-sensing is due to the static power dissipation. Repeaters on the other hand have very little static power and most of the power dissipated is dynamic or short-circuit power. In future technologies, timing critical low V_t devices are going to have a significant amount of leakage associated with them. Leakage power increases by more than an order of magnitude for BPTM models for 70nm technology as compared to 180nm. Since repeaters are usually very large, the amount of leak-

age power dissipated by repeaters is going to be significant. Power and other secondary issues[23] like noise, reliability and signal integrity need to be more thoroughly explored.

V. CONCLUSION AND FUTURE WORK

In this paper we looked at the impact of technology scaling on current-sensing and compared its performance with repeaters. The current-sensing technique provided significant gains over repeaters for the S-K model while for the BPTM model both techniques showed similar performances. After including the effect of inductance, differential current-sensing outperformed repeaters by significant amounts. If the clock frequency is aggressively scaled, current-sensing can drive longer lines as compared to repeaters. Based on this work, we make the following recommendations for the use of current-sensing:

- Current-sensing provides significant performance benefits (up to 50%) over repeaters (Figure 2) for small to medium length wires ($< 10 \text{ mm}$ for 0.18μ).
- If the S-K model of scaling is used then current-sensing wires can cover more area (with the gain increasing with scaling) as compared to repeaters (Figure 6) .
- The number of repeaters in a clock cycle is reducing (Figure 7), thus increasing the impact of sub-optimal placement. However their size is increasing to drive relatively more capacitive loads.
- For circuits where part of the clock cycle is taken up by logic or repeaters, current-sensing can be used to drive longer lines (typically the final segment to a latchFF) .

This comparison methodology and metrics can be used to compare other new interconnect circuit styles currently under development[6].

Future work involves evaluating the impact of current-sensing for realistic interconnect data (wire length, transition probability, criticality, topology) of some existing and proposed chips.

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